STRESS RELEASED IMAGE SENSOR PACKAGE STRUCTURE AND METHOD

RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 62/120,255 filed Feb. 24, 2015, and which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates to image sensors, and more particularly to an image sensor that is packaged in a manner that reduces induced stress.

BACKGROUND OF THE INVENTION

Silicon wafers are hard, brittle and stable. However, a silicon wafer is only stable before it is processed to form integrated circuits thereon (e.g. doping, processing, thinning, having layers of material/structure added to it, etc.). After that, the wafer will become unstable, can warp severely especially when the wafer is very thin and has unbalanced structural support, making the wafer extremely frail and susceptible to mechanical stress damage.

As the wafer diameter gets larger to enhance productivity/efficiency and chips get thinner to meet the requirements for heat dissipation, die stacking, reduced electrical resistance and low profile devices, such thin chips on large wafers will suffer ever-greater magnitude of stresses than ever before. These mechanical stress issues are especially severe for image sensor wafers (i.e. wafer on which image sensors are formed). The active side of an image sensor wafer has layers of material and structures formed thereon, which can include passivation, low-k dielectric layers, microlenses, color filters, conductive circuits, optical enhancements, light shielding, etc. These layers and structures not only make the silicon wafer unstable, they themselves are even more susceptible to the same mechanical stress and can become damaged.

Additionally, the active side of an image sensor wafer can be encapsulated with a protective substrate, which includes stand offs (dam) structures to space it from the wafer. The stand offs are bonded to the surface layer and introduce mechanical stress to the surface layer, together with the buildup of enormous amounts of mechanical stress during wafer thinning and dicing steps, which can cause cracking, delamination and many other defects on the surface layers and/or silicon substrate.

It is known in the art to make a pre-cut (partial dicing) to avert/release mechanical stress build up. Processing such as Dice Before Grinding (DBG) includes making a partial cut into the silicon wafer, thinning the other side of the wafer, using plasma etch to relieve stress build up in the wafer, and then making the final singulation cut. However, a limitation of DBG processing or similar processing is that such processing is for non-packaged semiconductor silicon wafers. What is needed is a method and structure for mechanical stresses relief that is compatible with and is part of the Wafer Level Packaging (WLP) process (i.e. packaging of the integrated circuits before wafer singulation).

BRIEF SUMMARY OF THE INVENTION

The aforementioned problems and needs are addressed by a sensor package that includes a first substrate with opposing first and second surfaces, a plurality of photo detectors formed on or under the first surface of the first substrate and configured to generate one or more signals in response to light incident on the first surface of the first substrate, a plurality of contact pads formed at the first surface of the first substrate and which are electrically coupled to the plurality of photo detectors, a plurality of holes each formed into the second surface of the first substrate and extending through the first substrate to one of the contact pads, and conductive leads each extending from one of the contact pads, through one of the plurality of holes, and along the second surface of the first substrate. The conductive leads are insulated from the first substrate. One or more trenches are formed into a periphery portion of the first substrate each extending from the second surface to the first surface. Insulation material covers sidewalls of the one or more trenches.

A method of forming a sensor package includes providing a sensor chip that includes a first substrate with opposing first and second surfaces, a plurality of photo detectors formed on or under the first surface of the first substrate and configured to generate one or more signals in response to light incident on the first surface of the first substrate, and a plurality of contact pads formed at the first surface of the first substrate and which are electrically coupled to the plurality of photo detectors. A plurality of holes are formed into the second surface of the first substrate, wherein each of the plurality of holes extends through the first substrate and to one of the contact pads. A plurality of conductive leads are formed each extending from one of the contact pads, through one of the plurality of holes, and along the second surface of the first substrate. One or more trenches are formed into a periphery portion of the first substrate each extending from the second surface to the first surface. Insulation material is formed that covers sidewalls of the one or more trenches.

A method of forming a plurality of sensor packages includes providing a sensor chip that includes a first substrate with opposing first and second surfaces, and a plurality of sensors formed thereon, wherein each sensor includes a plurality of photo detectors formed on or under the first surface of the first substrate and configured to generate one or more signals in response to light incident on the first surface of the first substrate, and a plurality of contact pads formed at the first surface of the first substrate and which are electrically coupled to the plurality of photo detectors. A plurality of holes are formed into the second surface of the first substrate, wherein each of the plurality of holes extends through the first substrate and to one of the contact pads. A plurality of conductive leads are formed each extending from one of the contact pads, through one of the plurality of holes, and along the second surface of the first substrate. A dam structure is formed on the first surface of the first substrate and around but not over the plurality of photo detectors. A second substrate is formed on the dam structure, wherein the second substrate extends over the plurality of photo detectors, and wherein the dam structure and the second substrate form a sealed cavity over the plurality of photo detectors for each of the sensors. One or more trenches are formed into the first substrate at a periphery portion of each of the sensors extending from the second surface, to the first surface, and into the dam structure. Insulation material is formed that covers sidewalls of the one or more trenches. The first substrate is singulated into separate die at the trenches, wherein each die includes one of the sensors.

Other objects and features of the present invention will become apparent by a review of the specification, claims and appended figures.